

WHAT IS CLAIMED IS:

1. A method of forming a vertical structure on a substrate, comprising the steps of:
selectively growing a first epitaxial layer of monocrystalline silicon on the substrate;
forming a layer of an insulative material over the first epitaxial layer;
removing a portion of the insulative layer to expose only a top surface of the first epitaxial layer;
selectively growing a second epitaxial layer of monocrystalline silicon on the exposed surface of the first epitaxial layer; and
forming a layer of an insulative material over the second epitaxial layer.
2. The method of Claim 1, further comprising repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height, each of the epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer of the vertical structure having insulated sidewalls and an insulated top surface.
3. The method of Claim 1, wherein the silicon substrate comprises monocrystalline silicon.
4. The method of Claim 1, wherein the silicon substrate comprises monocrystalline silicon having a (100) plane orientation.
5. The method of Claim 1, wherein at least one epitaxial layer is grown until a facet having a plane orientation of (100), (110), or (111) is formed on the top surface of the layer.
6. The method of Claim 1, wherein the epitaxial layers are grown until a facet having a plane orientation of (100) is formed on the top surface of the layers.
7. The method of Claim 1, wherein each epitaxial layer has a thickness of up to about 200 nm.

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8. The method of Claim 1, wherein one or more epitaxial layers has a thickness of about 70 to about 100 nm.
 9. The method of Claim 1, wherein the steps of selectively growing the epitaxial layers comprise introducing a silicon comprising gas over the substrate.
 10. The method of Claim 9, wherein the steps of selectively growing the epitaxial layers comprise:
 - heating the substrate to about 450°C to about 950°C; and
 - flowing at least one silicon comprising precursor gas over the substrate at a rate of about 10 to about 500 ccm, for about 15 to about 30 seconds.
 11. The method of Claim 10, wherein the silicon comprising gas is flowed over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at about 20 to about 40 nm/minute.
 12. The method of Claim 11, wherein the pressure is about 1 to about 20 Torr.
 13. The method of Claim 10, wherein the silicon comprising gas is flowed over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at less than about 10 nm/minute.
 14. The method of Claim 13, wherein the pressure is about 0.02 to less than about 1 Torr.
 15. The method of Claim 13, wherein the pressure is about 0.02 to less than about 1 Torr to provide a growth rate of the epitaxial layer at about 0.3 to less than about 10 nm/minute.

16. The method of Claim 9, wherein the silicon comprising gas is selected from the group consisting of silane combined with chlorine, disilane combined with chlorine, disilane combined with hydrochloric acid, dichlorosilane, silicon tetrachloride, and combinations thereof.
17. The method of Claim 9, wherein at least one of the steps of selectively growing the epitaxial layer comprises introducing the silicon comprising gas with a conductivity enhancing dopant.
18. The method of Claim 17, wherein the conductivity enhancing dopant is a p-type dopant.
19. The method of Claim 18, wherein the conductivity enhancing dopant is a p-type dopant selected from the group consisting of diborane, boron trichloride, boron trifluoride, and combinations thereof.
20. The method of Claim 17, wherein the conductivity enhancing dopant is an n-type dopant.
21. The method of Claim 20, wherein the conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphine, arsine, and combinations thereof.
22. The method of Claim 17, wherein the conductivity enhancing dopant is introduced at a variable rate to provide a concentration gradient of the dopant within the epitaxial layer.
23. The method of Claim 22, wherein the conductivity enhancing dopant is introduced at an increasing rate to provide a low to high concentration of the dopant within the epitaxial layer.

24. The method of Claim 2, further comprising doping the uppermost epitaxial layer by ion implantation.
25. The method of Claim 24, wherein the epitaxial layer is doped using a fluorine comprising gas selected from the group consisting of PF_3 , PF_5 , AsF_5 , and B^{11}F_3 .
26. The method of Claim 17, wherein the vertical structure is a source or drain having a height of at least about 10 to about 30 nm.
27. The method of Claim 1, further comprising, prior to the step of selectively growing the first epitaxial film, at least partially removing an oxide layer from the substrate.
28. The method of Claim 27, wherein the step of removing the oxide layer is by an oxide dry etch.
29. The method of Claim 28, wherein the oxide dry etch comprises exposing the substrate to an H_2 gas at about 800°C . to about 850°C .
30. The method of Claim 28, wherein the oxide dry etch comprises exposing the substrate to a reactive plasma at about 100°C .
31. The method of Claim 27, wherein the step of removing the oxide layer is by applying an oxide cleaning solution to the substrate.
32. The method of Claim 1, wherein the insulative layer comprises oxide, nitride, oxidized nitride, or a composite oxide/nitride.
33. The method of Claim 1, wherein the insulative layer comprises silicon nitride.

34. The method of Claim 33, wherein the insulative layer has a thickness of about 5 to about 20 nm.

35. The method of Claim 1, wherein the insulative layer comprises silicon oxide.

36. The method of Claim 35, wherein the insulative layer has a thickness of about 2 to about 5 nm.

37. The method of Claim 1, wherein at least one of the steps of forming the insulative layer is by annealing.

38. The method of Claim 37, wherein the annealing is by rapid thermal nitridation to form a nitride insulative layer.

39. The method of Claim 38, wherein the annealing by rapid thermal nitridation comprises exposing the epitaxial layer to ammonia or nitrogen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C.

40. The method of Claim 37, wherein the annealing is by rapid thermal oxidation to form an oxide insulative layer.

41. The method of Claim 40, wherein the annealing by rapid thermal oxidation comprises exposing the epitaxial layer to a dry oxygen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C.

42. The method of Claim 1, wherein at least one of the steps of removing the insulative layer is by reactive ion etching.

43. The method of Claim 42, wherein the reactive ion etching comprises exposing the insulative layer to an etch gas in an ionized state, the etch gas comprising at least one fluorine containing gas.

44. The method of Claim 1, wherein the vertical structure is formed adjacent to an existing gate or word line on the substrate.

45. The method of Claim 44, wherein the existing gate or word line is electrically isolated.

46. A method of forming a raised structure on a substrate, comprising the step of:
forming an epitaxial layer of monocrystalline silicon on the substrate;
forming a layer of insulative material over the epitaxial layer;
removing a portion of the insulative layer to leave only an exposed top surface of the epitaxial layer;
forming another epitaxial layer of monocrystalline silicon on the epitaxial layer; and
repeating the steps of forming the insulative layer, removing a portion of the insulative layer, and growing an epitaxial layer, until the vertical structure reaches a desired height, with the uppermost epitaxial layer having an insulated top surface.

47. A method of forming a vertical structure on a substrate, comprising forming multiple overlying epitaxial layers having insulated sidewalls and a top surface.

48. A method of forming a vertical structure on a substrate, comprising the steps of:
depositing a first epitaxial layer on the substrate, the first epitaxial layer comprising a horizontally oriented surface defining a facet;
forming a layer of an insulative material over the first epitaxial layer;
removing a portion of the insulative layer to expose the horizontal surface of the epitaxial layer;

depositing a second epitaxial layer on the exposed surface of the first epitaxial layer; the second epitaxial layer comprising a horizontally oriented surface defining a facet; and forming a layer of an insulative material over the second epitaxial layer.

49. The method of Claim 48, further comprising repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height.

50. A method of controlling growth of an epitaxial film to form a vertical structure on a substrate, comprising the steps of:

providing a substrate having an elevated structure disposed thereon, the elevated structure having an overlying insulative layer;

forming a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the elevated structure;

forming an insulative layer over the first epitaxial layer;

removing a horizontal surface of the insulative layer to expose only a top surface of the first epitaxial layer;

forming a second epitaxial layer of monocrystalline silicon over the first epitaxial layer; and

repeating the foregoing steps until the vertical structure is at a desired height.

51. The method of Claim 50, wherein the substrate has an overlying oxide layer, and the method further comprises prior to the step of depositing the first epitaxial layer, removing at least a portion of the oxide layer to expose the substrate.

52. The method of Claim 50, wherein the elevated structure is disposed on an area of microcrystalline silicon that is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

53. The method of Claim 52, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.
54. The method of Claim 50, wherein the vertical structure is a transistor gate.
55. The method of Claim 50, wherein the vertical structure is a source or drain, and at least one of the steps of forming the epitaxial layers is performed with a sufficiently high conductivity doping to effectively dope the source or drain.
56. The method of Claim 55, wherein the elevated structure adjacent to the source or drain is a transistor gate.
57. The method of Claim 55, wherein the vertical structure is a source or drain having a height of about 10 to about 30 nm.
58. A method of forming an elevated structure on a substrate in a semiconductor processing, comprising the steps of:
providing a semiconductor substrate comprising monocrystalline silicon;
growing a first epitaxial layer on the substrate until a horizontally oriented facet is formed;
forming an insulative layer over the first epitaxial layer;
removing the insulative layer to expose only a horizontal surface of the first epitaxial layer;
growing a second epitaxial layer on the first epitaxial layer until a horizontally oriented facet is formed; and
repeating the steps of forming the insulative layer, removing a portion of the insulative layer, and growing an epitaxial layer, until the elevated structure is at a desired height.

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59. The method of Claim 58, wherein the horizontally oriented facet of the first and second epitaxial layers has a (100) plane orientation.
60. A method of forming a raised structure on a silicon substrate, comprising the steps of:
selectively growing a first epitaxial layer of monocrystalline silicon on the substrate; forming a layer of an insulative material over the first epitaxial layer; and selectively growing one or more additional epitaxial layers of monocrystalline silicon to form the raised structure to a predetermined height, each epitaxial layer having insulated sidewalls and a top surface.
61. A method of fabricating an epitaxial structure on a substrate, comprising the steps of:
forming a first epitaxial layer of monocrystalline silicon on the substrate; annealing the epitaxial layer to form an insulative film thereover; etching the insulative film to expose only a horizontal surface of the first epitaxial layer; and repeating the foregoing steps to form additional overlying epitaxial layers until a vertical structure having a desired height is reached, the vertical structure comprising multiple epitaxial layers having only insulated sidewalls, with an uppermost epitaxial layer having insulated sidewalls and an insulated top surface.
62. The method of Claim 61, wherein the step of forming the epitaxial layer comprises heating the substrate and flowing a silicon comprising gas over the heated substrate.
63. The method of Claim 62, wherein the substrate is heated to about 450°C to about 950°C.
64. The method of Claim 62, wherein the gas is flowed over the substrate to provide a growth rate of the epitaxial layer at about 20 to about 40 nm/minute.

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65. The method of Claim 64, wherein the gas is flowed over the substrate at a flow rate of about 10 to about 500 cm³, and a pressure of about 1 to about 20 Torr.
66. The method of Claim 62, wherein the gas is flowed over the substrate to provide a growth rate of the epitaxial layer of less than about 10 nm/minute to about 0.3 nm/minute.
67. The method of Claim 66, wherein the gas is flowed over the substrate at a pressure of about 0.02 to less than 1 Torr.
68. The method of Claim 61, wherein the step of annealing is by rapid thermal nitridation to form a nitride insulative layer.
69. The method of Claim 61, wherein the step of annealing is by rapid thermal oxidation to form an oxide insulative layer.
70. The method of Claim 61, wherein the step of etching the insulative layer is by reactive ion etching.
71. The method of Claim 61, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.
72. A method for forming a DRAM cell on a silicon substrate, comprising the steps of:
forming a vertical gate structure on the substrate by the steps of:
 forming a first epitaxial layer of monocrystalline silicon on the substrate;
 forming a layer of an insulative material over the first epitaxial layer;
 removing a portion of the insulative layer to expose only a horizontal surface of
 the first epitaxial layer; and
 repeating the foregoing steps to form one or more additional overlying epitaxial
 layers until the gate structure is of a desired height, the gate structure
 comprising multiple overlying epitaxial layers having insulated sidewalls,

~~and an uppermost epitaxial layer having an insulated sidewalls and a horizontal surface; and~~

~~forming source and drain regions adjacent to the gate structure.~~

73. ~~The method of Claim 72, wherein the source and drain regions are elevated.~~

74. ~~The method of Claim 73, wherein the step of forming the source and drain regions comprises the steps of:~~

~~forming while doping, a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the gate structure;~~

~~forming a layer of an insulative material over the first epitaxial layer;~~

~~removing a portion of the insulative layer to expose only a horizontal surface of the first epitaxial layer;~~

~~repeating the foregoing steps to form one or more additional overlying epitaxial layers until the source and drain regions are of a desired height, the source and drain regions comprising multiple overlying epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer having insulated sidewalls and an insulated horizontal surface.~~

75. ~~The method of Claim 74, wherein the steps of forming the epitaxial layers comprise flowing a silicon comprising gas and a conductivity enhancing dopant over the substrate.~~

76. ~~The method of Claim 75, wherein the conductivity enhancing dopant is flowed at an increasing rate over time to provide a low to high concentration of the dopant within the epitaxial layer.~~

77. ~~The method of Claim 72, wherein the step of forming the source and drain regions comprises the steps of:~~

~~forming a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the gate structure;~~

~~forming a layer of an insulative material over the first epitaxial layer;~~

~~removing a portion of the insulative layer to expose only a horizontal surface of the first epitaxial layer;~~

~~repeating the foregoing steps to form multiple overlying epitaxial layers until the source and drain regions are of a desired height, the epitaxial layers having insulated sidewalls and an uppermost epitaxial layer having an exposed horizontal surface;~~

~~doping the uppermost epitaxial layer with a conductivity enhancing dopant by ion implantation; and~~

~~forming a layer of an insulative material over the uppermost epitaxial layer.~~

78. ~~The method of Claim 77, wherein the uppermost epitaxial layer is doped using a fluorine comprising gas selected from the group consisting of PF₃, PF₅, AsF₅, and B¹¹F₃.~~

79. ~~A method of forming an elevated source or drain structure on a substrate having a transistor gate disposed thereon, the method comprising the steps of:~~

~~selectively growing, while doping, a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the transistor gate;~~

~~depositing a layer of an insulative material onto the first epitaxial layer;~~

~~removing only the horizontal surface of the insulative layer;~~

~~growing additional overlying epitaxial layers according to the foregoing steps until the elevated source or drain structure reaches a desired height, each epitaxial layer having insulated sidewalls;~~

~~wherein, upon growing an uppermost epitaxial layer and depositing the insulative layer thereon, no removal step is performed such that the uppermost epitaxial layer comprises insulated sidewalls and an insulated horizontal surface.~~

80. ~~The method of Claim 79, wherein during the steps of selectively growing the epitaxial layers, a conductivity enhancing dopant is deposited at an increasing rate over time to provide a low to high concentration of the dopant within the epitaxial layer.~~

81. A method of forming an elevated source or drain structure on a substrate having a transistor gate formed thereon;
- selectively growing a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the gate;
- depositing a layer of an insulative material onto the first epitaxial layer;
- removing only the horizontal surface of the insulative layer;
- growing additional overlying epitaxial layers according to the foregoing steps until the elevated source or drain structure reaches a desired height; each epitaxial layer having insulated sidewalls and an uppermost epitaxial layer having an exposed top surface;
- doping the uppermost epitaxial layer with a conductivity enhancing dopant by ion implantation; and
- depositing a layer of an insulative material onto the uppermost epitaxial layer.
82. The method of Claim 81, wherein the uppermost epitaxial layer is doped using a fluorine comprising gas selected from the group consisting of PF_3 , PF_5 , AsF_5 , and B^{+}F_3 .
83. A method of forming an elevated transistor in a semiconductive wafer processing comprising the steps of:
- providing a semiconductor substrate;
- forming a buried drain in the substrate;
- forming an elevated gate over the buried drain by the steps of:
- forming a first epitaxial layer over the buried drain;
- forming an insulative layer over the first epitaxial layer;
- removing a portion of the insulative layer to expose only a horizontal surface of the first epitaxial layer;
- forming a second epitaxial layer over the first epitaxial layer;
- forming an insulative layer over the second epitaxial layer; and
- repeating the foregoing steps to form additional overlying epitaxial layers to form a pillar like structure having a desired height; each epitaxial

~~layer having insulated sidewalls, and the uppermost epitaxial layer having an exposed horizontal surface; and forming a source region onto the gate by forming at least one epitaxial layer over the uppermost epitaxial layer, while doping.~~

84. ~~The method of Claim 83, wherein the step of forming the buried drain comprises doping an area of the substrate with an n-type dopant.~~

85. ~~The method of Claim 84, wherein the substrate is doped by ion implantation.~~

86. ~~The method of Claim 84, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.~~

87. ~~The method of Claim 84, wherein the doped area of the substrate is about 50 nm to about 100 nm wide.~~

88. ~~The method of Claim 83, wherein the step of forming the source region comprises doping the at least one epitaxial layer with an n-type dopant.~~

89. ~~A method of semiconductive wafer processing, comprising forming an elevated transistor by the steps of:~~

~~providing a semiconductor substrate;~~
~~forming a buried drain in the substrate;~~
~~forming an elevated gate over the buried drain, the gate comprising multiple overlying epitaxial layers in a vertical orientation with each epitaxial layer having insulative sidewalls; and~~
~~forming a source region over the uppermost epitaxial layer of the gate, the source region comprising one or more epitaxial layers, each layer having insulative sidewalls and the uppermost layer having an insulated top surface.~~

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90. — The method of Claim 89, wherein the step of forming the elevated gate comprises:
~~depositing an epitaxial layer above the buried drain;~~
~~depositing a layer of insulative material over the epitaxial layer;~~
~~removing a horizontal surface of the insulative layer to expose the epitaxial layer;~~
and
~~repeating the foregoing steps until the gate reaches a desired height.~~
91. — The method of Claim 89, wherein the step of forming the source region comprises:
~~depositing an epitaxial layer onto an exposed horizontal surface of an uppermost epitaxial layer of the gate, while doping with a conductivity enhancing dopant.~~
92. — The method of Claim 91, wherein the conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphine, arsine, and combinations thereof.
93. — The method of Claim 89, wherein the step of forming the source region comprises:
~~depositing an epitaxial layer over an uppermost epitaxial layer, and doping the epitaxial layer of the gate with a conductivity enhancing dopant.~~
94. — The method of Claim 93, wherein the conductivity enhancing dopant is selected from the group consisting of PF₃, PF₅, AsF₅, and combinations thereof.
95. — The method of Claim 89, further comprising, prior to the step of forming the elevated gate, removing an oxide layer from the substrate overlying the buried drain.
96. — The method of Claim 89, wherein the step of forming the buried drain in the substrate comprises doping an area of the substrate with a conductivity enhancing dopant by ion implantation.
97. — The method of Claim 96, wherein the conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphine, arsine, and combinations thereof.

98. ~~The method of Claim 96, wherein the doped area of the substrate is about 50 nm to about 100 nm wide.~~

99. ~~The method of Claim 89, wherein a plurality of elevated transistors are formed on the substrate so as to define an array of transistors.~~

100. ~~The method of Claim 99, further comprising forming shallow trench isolation regions in the substrate to isolate the transistor.~~

101. A transistor in a semiconductor device, comprising:
source/drain diffusion regions formed on a semiconductive region of a substrate; and
a transistor gate formed on the semiconductive region between the source/drain diffusion regions, the transistor gate extending in a vertical orientation from the substrate, the transistor gate comprising at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost layer having an insulated top surface.

102. The transistor of Claim 101, wherein the source/drain diffusion regions are elevated and extend in a vertical orientation from the substrate surface adjacent to the transistor gate.

103. The transistor of Claim 102, wherein each of the source/drain diffusion regions comprise at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost layer having an insulated top surface.

104. The transistor of Claim 103, wherein the source/drain diffusion regions comprise an uppermost epitaxial layer comprising a conductivity enhancing dopant.

105. The transistor of Claim 103, wherein each of the epitaxial layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

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106. The transistor of Claim 101, wherein each epitaxial layer comprises a faceted top surface.
107. The transistor of Claim 101, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.
108. The transistor of Claim 101, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.
109. The method of Claim 108, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.
110. A transistor in a semiconductor device, comprising:
a transistor gate formed on a semiconductive region of a substrate; and
elevated source/drain diffusion regions formed on the semiconductive region adjacent to the transistor gate, and extending in a vertical plane from the substrate;
each of the source/drain diffusion regions covered by a layer of insulative material and comprising at least two overlying layers of epitaxially grown silicon.
111. The transistor of Claim 110, wherein the source/drain diffusion regions comprise an uppermost epitaxial layer comprising a conductivity enhancing dopant.
112. The transistor of Claim 110, wherein at least one of the epitaxial layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.
113. The transistor of Claim 112, wherein at least one of the epitaxial layers comprises a concentration gradient of the dopant.

114. The transistor of Claim 110, wherein the epitaxial layers comprise a faceted top surface.
115. The transistor of Claim 110, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.
116. The transistor of Claim 110, wherein the transistor gate is covered by a layer of insulative material and comprises at least two overlying layers of epitaxially grown silicon.
117. A transistor in a semiconductor device, comprising:
a substrate having a buried drain region;
a gate overlying the buried drain region, the gate comprising multiple, vertically-oriented and overlying epitaxial layers and a top surface, each epitaxial layer having insulated sidewalls;
a source region overlying the top surface of the gate, the source region comprising an epitaxial layer doped with a conductivity enhancing dopant, and covered by a layer of insulative material.
118. The transistor of Claim 117, wherein each of the epitaxial layers of the gate is about 50 to about 200 nm thick.
119. The transistor of Claim 117, wherein the epitaxial layer of the source region is at least about 10 nm thick.
120. The transistor of Claim 117, wherein the epitaxial layers have a faceted top surface.
121. The transistor of Claim 117, wherein the buried drain comprises an n-type conductivity enhancing dopant an n-type selected from the group consisting of phosphine, arsine, and combinations thereof.

122. The methodtransistor of Claim 117, wherein the buried drain region is about 50 nm to about 100 nm wide.

123. A transistor in a semiconductor device, comprising:
a transistor gate disposed on a semiconductive region of a substrate; and
an elevated source/drain diffusion region disposed on the substrate adjacent to the
transistor gate in a vertical orientation from the substrate; the source/drain diffusion region
comprising at least two overlying layers of epitaxially grown silicon; each epitaxial layer
having a top surface, and sidewalls with an overlying layer of an insulative material, and the
uppermost epitaxial layer having a top surface with an overlying layer of an insulative
material.

124. The transistor of Claim 123, wherein at least one of the epitaxial layers of the
source/drain diffusion region comprises a conductivity enhancing dopant.

125. The transistor of Claim 124, wherein the uppermost epitaxial layer of the
source/drain diffusion region comprises a conductivity enhancing dopant.

126. The transistor of Claim 124, wherein at least one of the epitaxial layers comprises a
concentration gradient of the dopant.

127. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises a
p-type dopant.

128. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises
an n-type dopant.

129. A semiconductor structure, comprising:

comprising at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

130. The semiconductor structure of Claim 129, wherein each epitaxial layer comprises a top surface defining a facet.

131. The semiconductor structure of Claim 130, wherein the facet has a (100) plane orientation.

132. The semiconductor structure of Claim 129, wherein each epitaxial layer has a thickness of up to about 200 nm.

133. The semiconductor structure of Claim 132, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.

134. The semiconductor structure of Claim 132, wherein one or more epitaxial layers has a thickness of about 70 to about 100 nm.

135. The semiconductor structure of Claim 132, wherein each epitaxial layer has a thickness of at least about 10 nm to about 30 nm.

136. The semiconductor structure of Claim 129, being disposed adjacent to a gate or word line.

137. The semiconductor structure of Claim 129, being disposed adjacent to a source/drain region.

138. The semiconductor structure of Claim 137, being a transistor gate.

139. The semiconductor structure of Claim 138, wherein the transistor gate is isolated within the substrate by at least one dielectric isolation region disposed in the substrate adjacent thereto.

140. The semiconductor structure of Claim 129, being a source/drain diffusion region.

141. The semiconductor structure of Claim 140, wherein the uppermost epitaxial layer comprises a conductivity enhancing dopant.

142. The semiconductor structure of Claim 140, wherein each of the epitaxial layers comprises a conductivity enhancing dopant.

143. A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material, an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

144. The semiconductor structure of Claim 143, wherein the insulative layer comprises an oxide film, a nitride film, an oxidized nitride film, or a composite oxide/nitride film.

145. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon nitride film.

146. The semiconductor structure of Claim 145, wherein the silicon nitride film has a thickness of about 5 to about 20 nm.

147. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon oxide film.

148. The semiconductor structure of Claim 147, wherein the silicon oxide film has a thickness of about 2 to about 5 nm.

149. A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material; an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; one or more of the epitaxial layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

150. The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises a p-type dopant.

151. The semiconductor structure of Claims 150, wherein the p-type dopant is selected from the group consisting of diborane, boron trichloride, and boron trifluoride, and combinations thereof.

152. The semiconductor structure of Claims 149, wherein the conductivity enhancing dopant comprises an n-type dopant.

153. The semiconductor structure of Claims 152, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

154. The semiconductor structure of Claims 149, wherein one or more of the epitaxial layers comprises a concentration gradient of the dopant within the epitaxial layer.

155. The semiconductor structure of Claims 154, wherein the concentration gradient comprises a low to high concentration of the dopant within the epitaxial layer, with the high dopant concentration at the top surface of the layer.